KSZ9021GN

Gigabit Ethernet Transceiver
with GMII/MII Support

KSZ9021GN-EVAL Board User's Guide

Revision 1.0 / January 2010
Revision 1.1 / Sept 2010

Revision History

Revision	Date	Summary of Changes
1.0	1/15/10	Initial Release
1.1	9/23/10	update to support GN rev A3, remove JP15, add R64. Separate TX_CLK and GTX_CLK

Table of Contents

List of Figures

List of Tables

1.0 Introduction

The KSZ9021GN is a completely integrated triple speed (10Base-T/100Base-TX/1000Base-T) Ethernet Physical Layer Transceiver for transmission and reception of data on standard CAT-5 unshielded twisted pair (UTP) cable.

The KSZ9021GN reduces board cost and simplifies board layout by using on-chip termination resistors for the four differential pairs and by integrating a LDO controller to drive a low cost MOSFET to supply the 1.2V core.

On the copper media interface, the KSZ9021GN can automatically detect and correct for differential pair misplacements and polarity reversals, and correct propagation delays and re-sync timing between the four differential pairs, as specified in the IEEE 802.3 standard for 1000Base-T operation.

The KSZ9021GN provides the industry standard GMII/MII (Gigabit Media Independent Interface / Media Independent Interface) for connection to GMII/MII MACs in Gigabit Ethernet Processors and Switches for data transfer at 1000 Mbps or 10/100Mbps speed.

The KSZ9021GN Socket Board (KSZ9021GN-EVAL) provides a comprehensive platform to evaluate the KSZ9021GN features. All KSZ9021GN configuration pins are accessible either by jumpers, test points or interface connectors.

2.0 Board Features

- Micrel KSZ9021GN 10Base-T/100Base-TX/1000Base-T Physical Layer Transceiver
- RJ-45 Jack for Ethernet cable interface
- Auto MDI/MDI-X for automatic detection and correction for straight-through and crossover cables
- GMII Loopback for standalone 1000Mbps evaluation
- MII Connector to interface with 10/100Mbps MAC controller/switch
- LED Indicators for link status and activity
- Jumpers to configure strapping pins
- Manual Reset Button for quick reboot after re-configuration of strapping pins
- USB port for MDC/MDIO programming access to KSZ9021GN PHY registers

3.0 Evaluation Kit Contents

The KSZ9021GN Evaluation Kit includes the following hardware:

- KSZ9021GN-EVAL Board (a.k.a. KSZ9021GN Socket Board)
- 5V DC Adapter

And a design package with the following collaterals:

- KSZ9021GN Socket Board Schematic (PDF and OrCAD DSN file)
- KSZ9021GN Socket Board Gerber Files
- KSZ9021GN Socket Board BOM
- KSZ9021GN Socket Board User's Guide (this document)
- KSZ9021GN IBIS Model
- Micrel MDIO Configuration Software

The latest KSZ9021GN Data Sheet is available from Micrel website.

4.0   Hardware Description

The KSZ9021GN-EVAL board is the evaluation platform for the KSZ9021GN Gigabit Ethernet Transceiver. Configuration of the KSZ9021GN is accomplished through on-board jumper selections and/or by PHY register access via the KSZ9021GN MDC/MDIO management pins via the USB port (CN1).
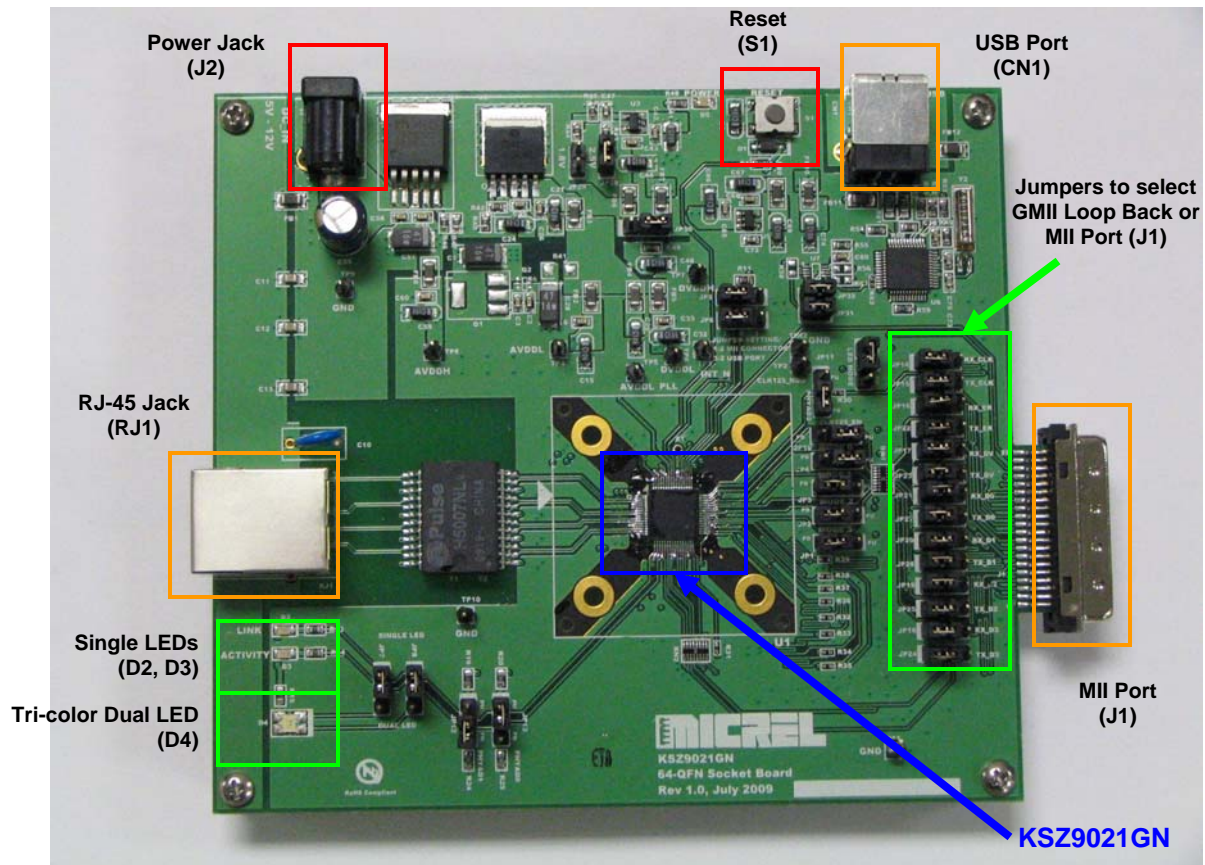
Figure 1. KSZ9021GN-EVAL Board

Features include a RJ-45 Jack for 10/100/1000 Ethernet speed cable connection, programmable LED indicators for reporting link status and activity, and a manual reset button for quick reboot after re-configuration of strapping pins.

GMII receive output clock and signals can be looped back to GMII transmit input clock and signals to provide a standalone platform to evaluate the KSZ9021GN device in 1000Mbps mode.

MII Port (J1) provides the 10/100 MAC interface connections to Micrel KSZ88xx 3-port Switch evaluation boards with the mating MII MAC interface connectors.

The KSZ9021GN-EVAL board receives power from a DC power jack (J2). A 5V DC power adapter is provided with the board. Any DC power adapter in the range of 5V to 12V with a current rating of 2 Amp or better can also be used.

4.1   Jumper Setting & Definition

At power-up, the KSZ9021GN device is configured via strapping pins that are set by external pull-up and pull-down resistors. The KSZ9021GN-EVAL board provides jumpers for the KSZ9021GN device strap-in settings and for selective board options.

Jumpers allow for quick configuration and re-configuration. To override the current KSZ9021GN device and board settings, simply select and close the desired jumper setting(s) and toggle the on-board manual reset button (S1) for the new setting(s) to take effect.

The KSZ9021GN-EVAL board jumper settings are defined in the table below.

Jumper	KSZ9021GN Pin Name	Setting	Function
KSZ9021GN Device Strapping Pins			
JP1	MODE3	Close pins (1, 2)	Set MODE3 = 1
		Close pins (2, 3)	Set MODE3 = 0
JP2	MODE2	Close pins (1, 2)	Set MODE2 = 1
		Close pins (2, 3)	Set MODE2 = 0
JP3	MODE1	Close pins (1, 2)	Set MODE1 = 1
		Close pins (2, 3)	Set MODE1 = 0
JP4	MODE0	Close pins (1, 2)	Set MODE0 = 1
		Close pins (2, 3)	Set MODE0 = 0
JP11	PHYAD2	Close pins (1, 2)	Set PHYAD2 = 1
		Close pins (2, 3)	Set PHYAD2 = 0
JP12	PHYAD1	Close pins (1, 2)	Set PHYAD1 = 1
		Close pins (2, 3)	Set PHYAD1 = 0
JP13	PHYAD0	Close pins (1, 2)	Set PHYAD0 = 1
		Close pins (2, 3)	Set PHYAD0 = 0
JP10	CLK125_EN	Close pins (1, 2)	Enable 125 MHz Clock Output
		Close pins (2, 3)	Disable 125 MHz Clock Output
JP9	LED_MODE	Close pins (1, 2)	Select Single LED Mode
		Close pins (2, 3)	Select Tri-color Dual LED Mode
KSZ9021GN-EVAL Board Settings			
JP7	LED2	Close pins (1, 2)	Use for Single LED Mode
		Close pins (2, 3)	Use for Tri-color Dual LED Mode
JP8	LED1	Close pins (1, 2)	Use for Single LED Mode
		Close pins (2, 3)	Use for Tri-color Dual LED Mode
JP6	MDC	Close pins (1, 2)	Select MDC clock to MII Port (J1)
		Close pins (2, 3)	Select MDC clock to USB Controller (U6)
JP5	MDIO	Close pins (1, 2)	Select MDIO signal to MII Port (J1)
		Close pins (2, 3)	Select MDIO signal to USB Controller (U6)
JP14	RX_CLK	Close pins (1, 2)	Select GMII GTX_CLK clock for GMII Loop Back
		Close pins (2, 3)	Select MII RX_CLK clock to MII Port (J1)
JP16	RX_ER	Close pins (1, 2)	Select GMII TX_ER signal for GMII Loop Back
		Close pins (2, 3)	Select MII RX_ER signal to MII Port (J1)

Jumper	KSZ9021GN Pin Name	Setting	Function
JP17	RX_DV	Close pins (1, 2)	Select GMII TX_EN signal for GMII Loop Back
		Close pins (2, 3)	Select MII RX_DV signal to MII Port (J1)
JP18	RXD3	Close pins (1, 2)	Select GMII TXD3 signal for GMII Loop Back
		Close pins (2, 3)	Select MII RXD3 signal to MII Port (J1)
JP19	RXD2	Close pins (1, 2)	Select GMII TXD2 signal for GMII Loop Back
		Close pins (2, 3)	Select MII RXD2 signal to MII Port (J1)
JP20	RXD1	Close pins (1, 2)	Select GMII TXD1 signal for GMII Loop Back
		Close pins (2, 3)	Select MII RXD1 signal to MII Port (J1)
JP21	RXD0	Close pins (1, 2)	Select GMII TXD0 signal for GMII Loop Back
		Close pins (2, 3)	Select MII RXD0 signal to MII Port (J1)
JP22	TX_ER	Close pins (1, 2)	Select GMII RX_ER signal for GMII Loop Back
		Close pins (2, 3)	Select MII TX_ER signal to MII Port (J1)
JP23	TX_EN	Close pins (1, 2)	Select GMII RX_DV signal for GMII Loop Back
		Close pins (2, 3)	Select MII TX_EN signal to MII Port (J1)
JP24	TXD3	Close pins (1, 2)	Select GMII RXD3 signal for GMII Loop Back
		Close pins (2, 3)	Select MII TXD3 signal to MII Port (J1)
JP25	TXD2	Close pins (1, 2)	Select GMII RXD2 signal for GMII Loop Back
		Close pins (2, 3)	Select MII TXD2 signal to MII Port (J1)
JP26	TXD1	Close pins (1, 2)	Select GMII RXD1 signal for GMII Loop Back
		Close pins (2, 3)	Select MII TXD1 signal to MII Port (J1)
JP27	TXD0	Close pins (1, 2)	Select GMII RXD0 signal for GMII Loop Back
		Close pins (2, 3)	Select MII TXD0 signal to MII Port (J1)
JP28	Reserved – not used		
JP29	Reserved – not used		
JP30	DVDDH	Pins (1, 2)	Reserved – always leave open
		Close pins (2, 3)	Select 3.3V for KSZ9021GN digital I/Os
JP31 [1]	MDC	Close Jumper	Close MDC clock to USB Controller (U6)
		Open Jumper	Open MDC clock to USB Controller (U6)
JP32 [1]	MDIO	Close Jumper	Close MDIO signal to USB Controller (U6)
		Open Jumper	Open MDIO signal to USB Controller (U6)

Note: [1] JP31 and JP32 connect the MDC/MDIO signals to U6 when U7 is not populated.

Table 1. KSZ9021GN-EVAL Board – Jumper Definition

The following table lists the strapping pin definitions for the KSZ9021GN-EVAL board jumpers.

Jumper	Pin	Pin Name	Pin Function
JP1 JP2 JP3 JP4	39 41 43 44	MODE3 MODE2 MODE1 MODE0	The MODE[3:0] strap-in pins are latched at power-up / reset and are defined as follows: <table><tr><td>**MODE[3:0]**</td><td>**Mode**</td></tr><tr><td>0001</td><td>GMII / MII</td></tr><tr><td>0100</td><td>NAND Tree</td></tr><tr><td>0111</td><td>Chip Power Down</td></tr></table> All other MODE[3:0] settings not listed are reserved and are not used by the KSZ9021GN-EVAL. **MODE[3:0] = 0001 is set as the default for the board.**
JP11 JP12 JP13	48 17 19	PHYAD2 PHYAD1 PHYAD0	The PHY Address is latched at power-up / reset and is configurable to any value from 1 to 7. PHY Address bits [4:3] are always set to '00'. **PHYAD[2:0] = 001 is set as the default for the board.**

JP10	45	CLK125_EN	CLK125_EN is latched at power-up / reset and is defined as follows:
			    Pull-up (1) = Enable 125MHz Clock Output
			    Pull-down (0) = Disable 125MHz Clock Output
			Pin 56 (CLK125_NDO) provides the 125MHz reference clock output option for use by the MAC.
			
			CLK125_EN = 0 is set as the default for the board.

JP9	56	LED_MODE	LED_MODE is latched at power-up / reset and is defined as follows:
			    Pull-up (1) = Single LED Mode
			    Pull-down (0) = Tri-color Dual LED Mode
			
			LED_MODE = 1 is set as the default for the board.

Table 2. Strapping Pin Definitions for KSZ9021GN-EVAL Board Jumpers

4.2   Test Point Definition

The KSZ9021GN-EVAL board has 12 usable test points, as defined in the following table.

Test Point	Definition
TP1	XI Clock Input (KSZ9021GN pin 61)
TP2	CLK125_NDO Clock Output (KSZ9021GN pin 56)
TP3	Interrupt Signal (KSZ9021GN pin 53) with 4.7K external pull-up
TP4	AVDDL voltage – KSZ9021GN power pins
TP5	AVDDL_PLL voltage – KSZ9021GN power pin
TP6	DVDDL voltage – KSZ9021GN power pins
TP7	DVDDH voltage – KSZ9021GN power pins
TP8	AVDDH voltage – KSZ9021GN power pins
TP9	Signal Ground
TP10	Signal Ground
TP11	Signal Ground
TP12	Signal Ground

Table 3. KSZ9021GN-EVAL Board – Test Point Definition

4.3   RJ-45 Copper Interface

The RJ-45 copper interface (RJ1) connects to standard unshielded twisted pair (UTP) CAT-5 Ethernet cable to interface with 10Base-T/100Base-TX/1000Base-T network devices.

The KSZ9021GN copper media interface can automatically detect and correct for differential pair misplacements and polarity reversals, and correct propagation delays and re-sync timing between the four differential pairs, as specified in the IEEE 802.3 standard for 1000Base-T operation.

Auto MDI/MDI-X is supported for automatic detection and correction for straight and crossover cables when interfacing to link partners with fixed MDI or MDI-X setting.

4.4   LED Indicators

The KSZ9021GN device provides two programmable LED output pins, LED2 (pin 17) and LED1 (pin 19). On the KSZ9021GN-EVAL board, these two LED pins are connected to two sets of LEDs to support two LED configurations: Single LED mode and Tri-color Dual LED mode.

4.4.1   Single LED Mode

To enable Single LED mode,

- Close pins (1, 2) of jumpers JP7 and JP8 to select D2 and D3, respectively for the single LEDs.
- Close pins (1, 2) of jumper JP9 to set the LED_MODE strap-in for Single LED mode.
- Power-up the board.

After board power-up, the on-board D2 and D3 LEDs are defined as follows:

LED	LED Definition	Link / Activity
D2	OFF	Link off
	Green – ON	Link on (any speed)
D3	OFF	No Activity
	Green – Blinking	Activity (RX, TX)

Table 4: Single LED Mode – LED Definition

4.4.2 Tri-color Dual LED Mode

To enable Tri-color Dual LED mode,
- Close pins (2, 3) of jumpers JP7 and JP8 to select D4 for the tri-color dual LED.
- Close pins (2, 3) of jumper JP9 to set the LED_MODE strap-in for Tri-color Dual LED mode.
- Power-up the board.

After board power-up, the on-board D4 LED is defined as follows:

LED: D4	Link / Activity
OFF	Link off
Green – ON	1000Mbps Link / No Activity
Green – Blinking	1000Mbps Link / Activity (RX, TX)
Red – ON	100Mbps Link / No Activity
Red – Blinking	100Mbps Link / Activity (RX, TX)
Orange – ON	10Mbps Link / No Activity
Orange – Blinking	10Mbps Link / Activity (RX, TX)

Table 5: Tri-color Dual LED Mode – LED Definition

4.5 Gigabit Media Independent Interface (GMII)

The KSZ9021GN-EVAL Board is shipped with the GMII signals configured for GMII Loop Back. Pins 1 and 2 of jumpers [JP14—JP27] are closed to connect the GMII output clock and signals to their respective GMII input clock and signals. Refer to KSZ9021GN Socket Board Schematic for details.

GMII Loop Back enables the KSZ9021GN device to operate on a standalone evaluation platform without the need of an external GMAC for 1000Mbps mode operation. Gigabit (1000Base-T) Ethernet traffic from the link partner (Spirent SmartBits 6000B in the following figure) is received by the KSZ9021GN device, looped back externally via GMII pins and jumpers [JP14—JP27], and transmitted back to the link partner.
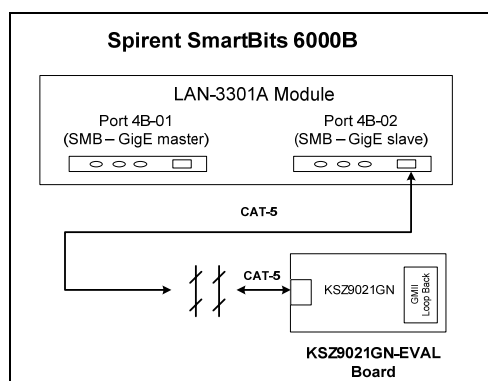

Figure 2. KSZ9021GN-EVAL Board – GMII Loop Back

4.6 Media Independent Interface (MII)

The KSZ9021GN-EVAL Board provides access to the MII clocks and signals at the MII Port (J1). Pins 2 and 3 of jumpers [JP14—JP27] are closed to connect the MII clocks and signals from the KSZ9021GN device to the MII Port (J1). Similarly, pins 1 and 2 of jumpers [JP6, JP5] are closed to connect the MII Management pins (MDC, MDIO) from the KSZ9021GN device to the MII Port (J1). Refer to KSZ9021GN Socket Board Schematic for details.

The following figure shows the KSZ9021GN-EVAL Board attached to Spirent SmartBits (Ethernet traffic generator/analyzer) for testing. MII Port (J1) provides the 10/100 MAC interface and plugs directly into the connector of the SX-7210 Module, while the RJ-45 connector (RJ1) provides the 10/100 copper interface and is connected via CAT-5 Ethernet cable to the SX-7410 Module.
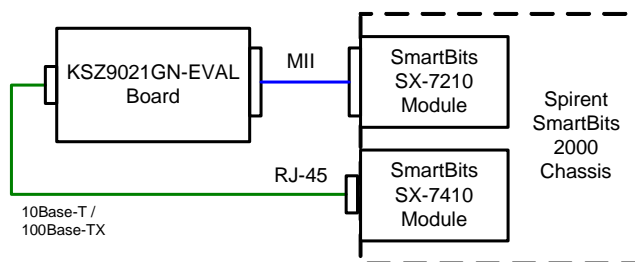

Figure 3. KSZ9021GN-EVAL Board – MII Interface Connection with Spirent SmartBits

The Micrel KSZ88xx 3-port Switch evaluation boards have the corresponding 10/100 MII MAC interface connectors that plug directly into the MII Port (J1) of the KSZ9021GN-EVAL Board to provide an end-to-end 10/100 copper to 10/100 copper evaluation platform.

The MII Port (J1) is a 40-pin male edge connector that interfaces with and plugs directly into the mating AMP 787170-4 (40-pin, right angle, female) connector

The following table lists the pin outs for the MII Port (J1).

Pin #	Signal	Pin #	Signal
1	VCC (NC)	21	VCC (NC)
2	MDIO	22	Ground
3	MDC	23	Ground
4	RXD3	24	Ground
5	RXD2	25	Ground
6	RXD1	26	Ground
7	RXD0	27	Ground
8	RX_DV	28	Ground
9	RX_CLK	29	Ground
10	RX_ER	30	Ground
11	TX_ER	31	Ground
12	TX_CLK	32	Ground
13	TX_EN	33	Ground
14	TXD0	34	Ground
15	TXD1	35	Ground
16	TXD2	36	Ground
17	TXD3	37	Ground
18	COL	38	Ground
19	CRS	39	Ground
20	VCC (NC)	40	VCC (NC)

Table 6. MII Port (J1) – MII Pin Definition

4.7   USB Port

The USB port (CN1) provides programming access to the KSZ9021GN device's PHY registers through its MDC/MDIO management pins.

See following software section for PHY register access.

5.0   MicrelMdioConfig Software – Installation

The Micrel MDIO Configuration Software (**MicrelMdioConfig**) runs on a PC with the Window XP Operating System. It communicates to the KSZ9021GN-EVAL board via USB to provide programming access to the KSZ9021GN device's PHY registers.

The Micrel software is provided in a Microsoft Windows Installer installation package file (*.msi file) with the following file name.

> **MicrelMdioConfig_verx.xx.msi**   // where x.xx is the release version number

5.1   MicrelMdioConfig Installation

Before running the **MicrelMdioConfig** installation, make sure previously installed version of the **MicrelMdioConfig** software has been removed and the USB cable to the KSZ9021GN-EVAL board is unplugged.

To unpack the **MicrelMdioConfig_verx.xx.msi** file and start the installation, double click on the file name from Windows Explorer, and proceed with the following steps:
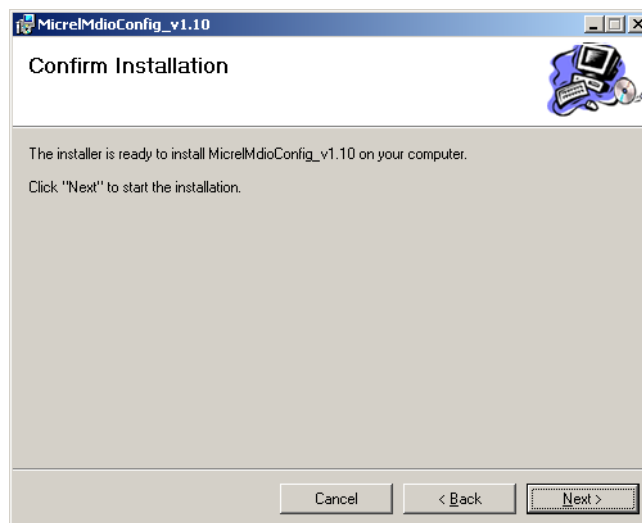
1.   At the "**Welcome"** screen, press the **Next>** button.
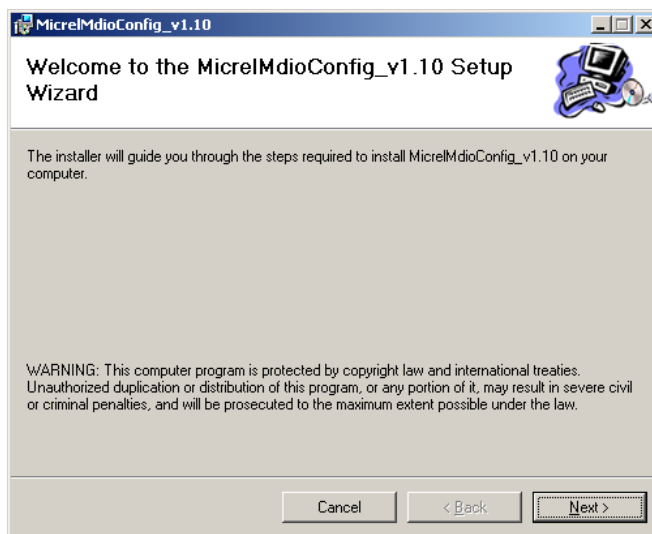
2. At the "**Select Installation Folder**" screen,

    a. Select the folder for the software installation (c:\MicrelMDIOConfig\ is the default installation folder).
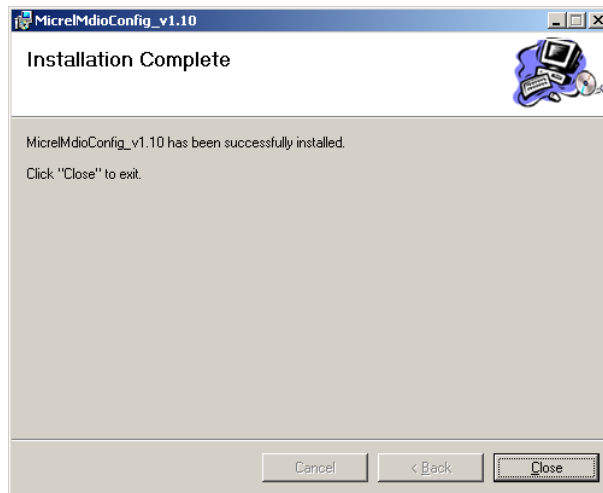
    b. Press the **Next>** button.
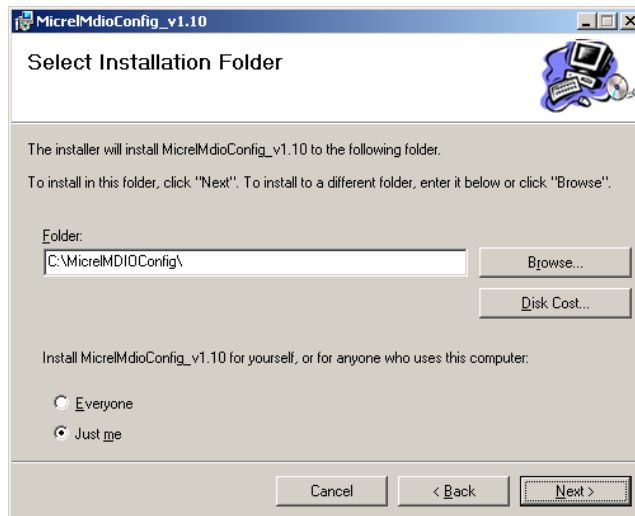
3. At the "**Confirm Installation**" screen,

    a. Press the **Next>** button for the installation to proceed.

    b. Wait a few seconds for the installation to finish.

4. When the installation is finished, the "**Installation Complete**" screen is returned. Press the **Close>** button to exit.

After the **MicrelMdioConfig** software installation, an installation folder (c:\MicrelMDIOConfig\ is the default installation folder) is created containing the **MicrelMdioConfig** application programs and software drivers for the KSZ9021GN-EVAL board's USB port. Also, a shortcut is created on the Windows Desktop for the Windows GUI program, **MicrelMdioConfigWinApp.exe**.
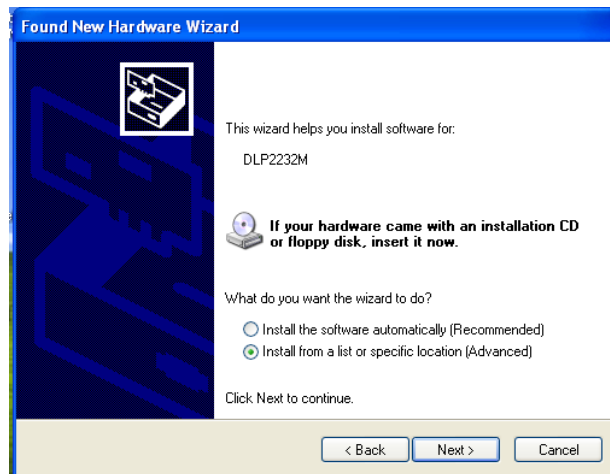
5.2   USB Driver Installation

Before installing the USB driver, complete the **MicrelMdioConfig** software installation in the previous section to extract the USB driver from the **MicrelMdioConfig_verx.xx.msi** installation file and have it copied to the created installation folder.

Power-up the KSZ9021GN-EVAL board and connect an USB cable from the board to the PC to initiate the USB driver installation, and proceed with the following steps:

1. Windows XP detects the KSZ9021GN-EVAL board's USB device. At the "**Welcome to the Found New Hardware Wizard**" screen,

    a.   Select "**No, not this time".**

    b.   Press the **Next>** button.

2. At the "**… install software for:**" screen,

    a. Select "**Install from a list or specific location (Advanced)".**

    b. Press the **Next>** button.

3. At the "**Please choose your search and installation options"** screen,

    a. Select **"Include this location in the search:"**

    b. Press the **Browse** button and navigate to and select the USB driver directory (**C:\MicrelMDIOConfig\D2XXDriver\CDM 2.02.04 WHQL Certified** is the USB driver directory for the default installation folder).

    c. Press the **Next>** button for the USB driver installation to proceed.

    d. Wait for the USB driver installation to finish.

---
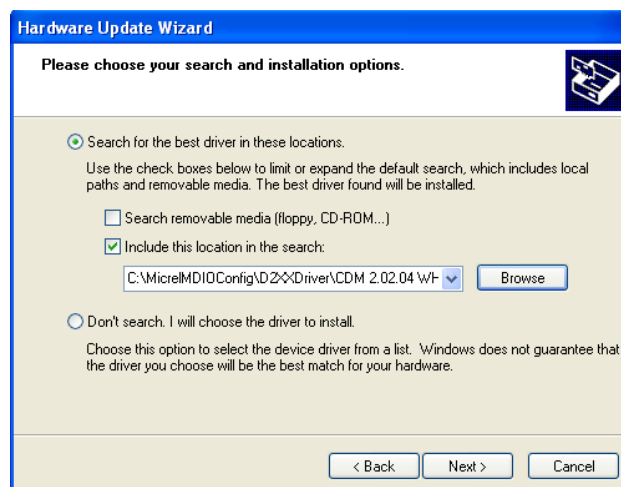
4. At the "**Completing the Found New Hardware Wizard"** screen, press the **Finish** button to close the wizard and exit.

5. After the USB driver installation, verify the USB driver is installed.

    a. Go to the **Windows XP System Properties** box (select the System icon under Windows Start Menu -> Settings -> Control Panel).
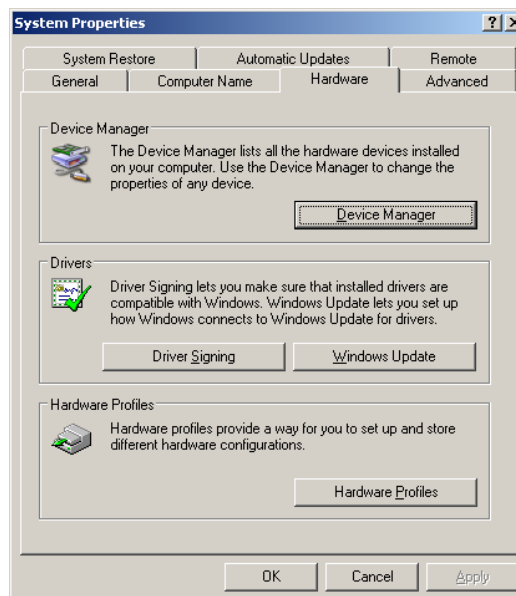
b. Press the **Device Manager** button

c. Scroll down to the end of Universal Serial Bus controllers to verify "**USB Serial Converter A**" and "**USB Serial Converter B**" are installed.
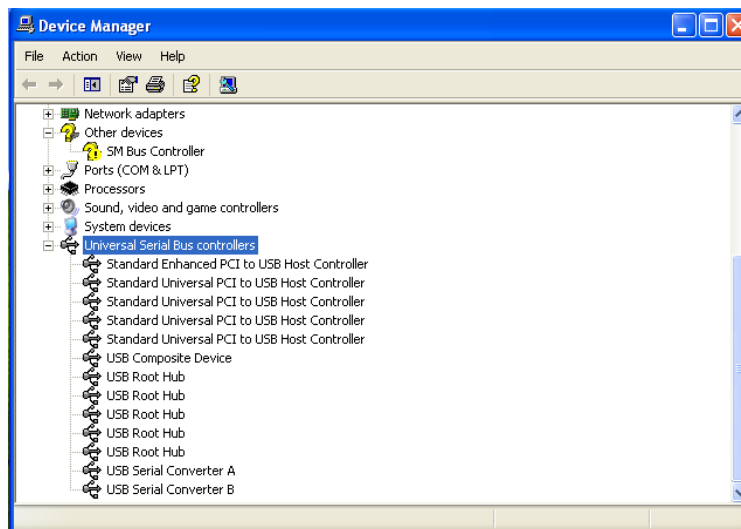
6.0   MicrelMdioConfig Software – Application Programs

The **MicrelMdioConfig** application programs reside in the software installation folder created in the previous section (c:\MicrelMDIOConfig\ is the default installation folder). In the folder, there are two application programs that can be used to access the KSZ9021GN device's PHY registers:

- **MicrelMDIOConfigWinApp.exe**   // Windows GUI program
- **mdioConfig.exe**   // Windows Command Prompt program

Both programs can be opened concurrently. Use the Windows Task Bar to switch between the two programs.

6.1   Windows GUI program

The **MicrelMDIOConfigWinApp.exe** program is the Windows graphical user interface program.

### 6.1.1   Running the program

To launch the program, double click on either the **MicrelMDIOConfigWinApp.exe** file name from Windows Explorer or the Shortcut created for the program on the Windows Desktop, and proceed with the following steps:

1.   At the configuration menu screen,

   a.   Select "**KSZ9021 Gigabit Ethernet Transceiver"** for the device to configure.

   b.   Set the "**Device Address**" to the KSZ9021GN-EVAL board's PHY address.

   c.   Use the "**Pre-config file"** button to load PHY configuration script file (if any). More detail in following sub-section.

   d.   Use the default DeviceID value or enter a new value (if the KSZ9021GN DeviceID in PHY registers 2 and 3 is different).

   e.   Press the **Next>** button to continue.
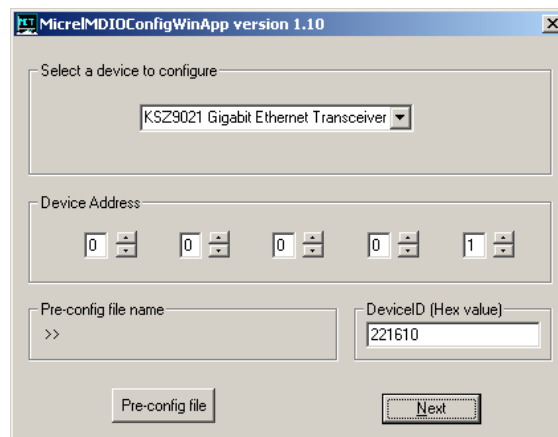
Figure 4. MicrelMDIOConfigWinApp Program – Configuration Menu Screen

---

Micrel, Inc.   January 15, 2010
                                                                                                                           Rev. 1.0

2. At the program menu screen,

    a. Use the tabs across the top to select **Reg 0-3**, **Reg 4-7**, etc.
        i. *Registers 256 and 258-261 are not used by the KSZ9021GN. The default values in these registers should not be changed.*

    b. To read the PHY registers,
        i. Press the **Read** button to refresh the register values in the program.

    c. To write to the PHY register(s),
        i. Use the register bit check box to set the bit(s) to "1" (checked) or "0" (unchecked).
        ii. Press the **Write** button.
        iii. Press the **OK** button to continue when the following "**Write Successful**" prompt is returned.
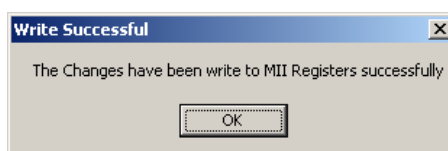
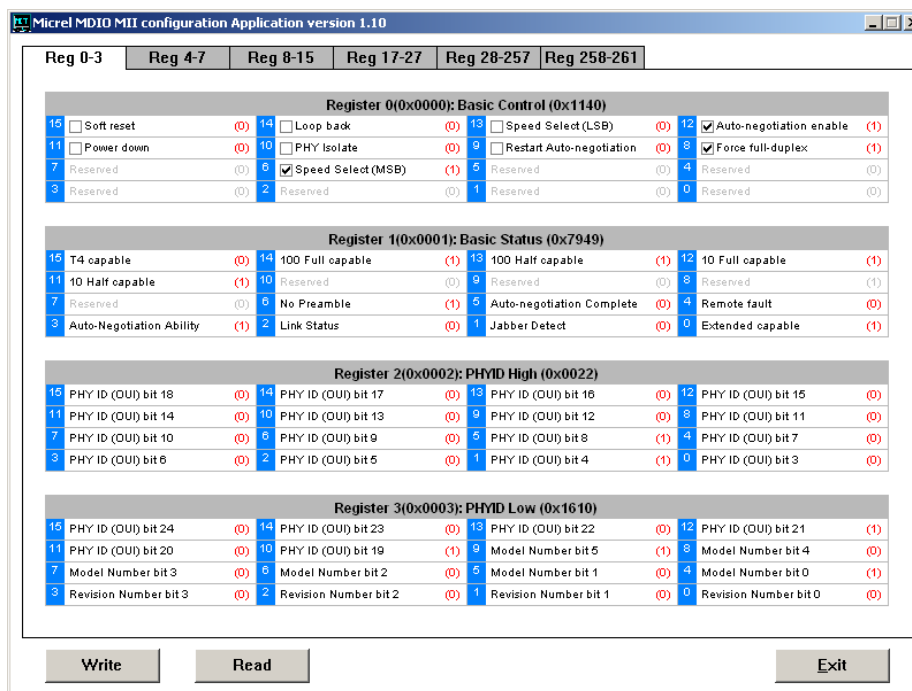   d. Press the **Exit** button to close and exit the program.

Figure 5. MicrelMDIOConfigWinApp Program – Program Menu Screen


6.1.2   Creating and Loading Script Files

The PHY configuration script file for the **MicrelMDIOConfigWinApp.exe** program is a text file with the *.mdo file name extension. A sample file, pre-config.mdo, is loaded in the program folder during the software installation. The sample file contains the following script:

> #command syntax: [w|iw] [register address (hex)] [write value (hex)]
> #w 0x0 0x1140
> #iw 0x104 0xc0c0
> #iw 0x105 0x7777

Where the parameters are defined as follows:

#	: # symbol precedes line for comment or removal
w	: Direct register write for KSZ9021GN's IEEE Defined and Vendor Specific Registers
iw	: Indirect register write for KSZ9021GN's Extended Registers.

The PHY configuration script file for the **MicrelMDIOConfigWinApp.exe** program is loaded at the configuration menu during program start-up. Use the "**Pre-config file**" button to load the *.mdo PHY configuration script file, as shown in the following figure.
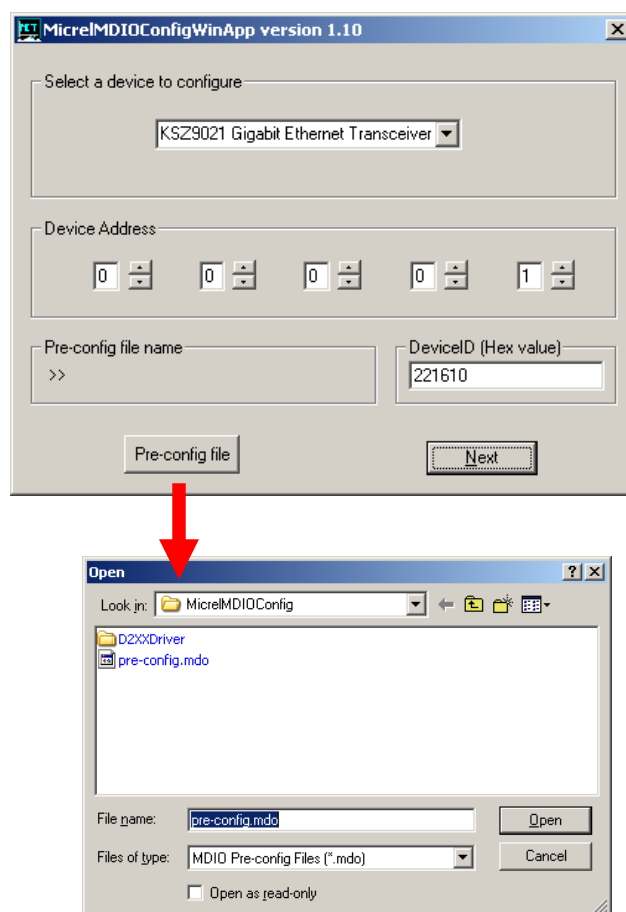
Figure 6. MicrelMDIOConfigWinApp Program – Pre-config Script File Loading

Micrel, Inc.   January 15, 2010
                                                                                      Rev. 1.0

6.2   Windows Command Prompt – Command Line program

The **mdioConfig.exe** program is the command line interface program.

6.2.1   Running the program

The **mdioConfig.exe** program resides in the software installation folder created during the software installation (c:\MicrelMDIOConfig\ is the default installation folder). The program reads in the PHY address from the **deviceinfo.txt** file every time it is executed.

The **deviceinfo.txt** file is loaded in the program folder during the software installation, and has the PHY address set to "1", as the default. If the KSZ9021GN-EVAL board is set to a different PHY address, modify the hex PHY address value accordingly for the following line in the **deviceinfo.txt** file.

        address=0x0001

The **mdioConfig.exe** program is executed from a Windows Command Prompt. Open a Windows Command Prompt (select the Command Prompt under Windows Start Menu -> Programs -> Accessories) and navigate to the **mdioConfig.exe** program directory (c:\MicrelMDIOConfig\ is the program directory for the default installation folder), as shown in the following figure.
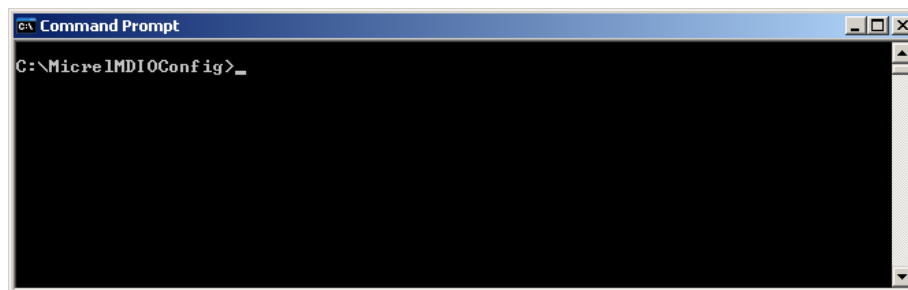

Figure 7. mdioConfig Program – Windows Command Prompt

The **mdioConfig.exe** program is started by typing the **mdioConfig.exe** program name at the Windows Command Prompt and pressing the **ENTER** key. Next, the program displays instruction for direct register read/write, indirect register read/write and to exit the program. Follow the instruction, as shown in the following figure, for the desired action.
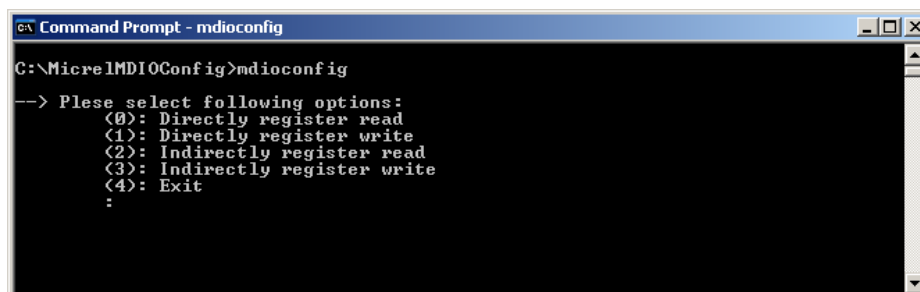

Figure 8. mdioConfig Program – in operation

6.2.2   Creating and Loading Script Files

The **mdioConfig.exe** program can execute with all parameters placed in a single command line, as shown in the following examples:

Direct Register Read
>> **mdioconfig r** [register address (hex)]
>> **mdioconfig r 0x0000**

Direct Register Write
>> **mdioconfig w** [register address (hex)] [write value (hex)]
>> **mdioconfig w 0x0000 0x1940**

Indirect Register Read
>> **mdioconfig ir** [register address (hex)]
>> **mdioconfig ir 0x0101**

Indirect Register Write
>> **mdioconfig iw** [register address (hex)] [write value (hex)]
>> **mdioconfig iw 0x0102 0x0011**

Where the parameters are defined as follows:

r	: Direct register read for KSZ9021GN's IEEE Defined and Vendor Specific Registers
w	: Direct register write for KSZ9021GN's IEEE Defined and Vendor Specific Registers
ir	: Indirect register read for KSZ9021GN's Extended Registers
iw	: Indirect register write for KSZ9021GN's Extended Registers

A group of single command lines can be put in a batch file (*.bat) to produce a PHY configuration script file. The following Windows Command Prompt capture shows the four examples above run in a script file, "example.bat."

Figure 9. mdioConfig Program – script file "example.bat" run

When the single command line is executed, each direct/indirect register read back is dumped and appended to a log file, "mdiolog.txt."